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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,448	04/01/2004	Soon-Hong Ahn	8021-227 (SS-19246-US)	7782

22150 7590 06/17/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,448	AHN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6-10, 19, 23-24 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 5889309 to Yu et al.

Regarding claims 1, Yu discloses a semiconductor device in fig. 9 comprising: a first well 60, column 5 line 22, connected to a pad 10, column 4 line 5, to which an external pin is connected, the first well 60 including a first-type diffusion region 46, column 4 line 62, that receives a well bias voltage V_{dd}, fig. 9; a second well 50, column 4 line 3, adjacent to the first well 60, the second well 50 including an insulating region 54 and at least one second-type diffusion region 52, fig. 9, outside the insulating region 54, fig. 9; and a third well 60 adjacent to the second well 50 and including a first-type diffusion region 48 that receives a first voltage V_dd, wherein the insulating region inside the second well along with the first-type diffusion region of the first well constitute a bipolar junction transistor, column 2 line 30 fig. 4, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure

recited in the Yu's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 6, Yu discloses the semiconductor device of claim 1, wherein the first and third wells 60s are N-wells, fig. 9.

Regarding claim 7, Yu discloses the semiconductor device of claim 1, wherein the well bias voltage applied to the first-type diffusion region 46 of the first well 60 is a power supply voltage, fig. 9.

Regarding claim 8, Yu discloses the semiconductor device of claim 1, wherein a region to which the pad 10 is connected is a second-type diffusion region 44, fig. 9.

Regarding claim 9, Yu discloses the semiconductor device of claim 1, wherein the first-type diffusion regions 46 are formed of N-type impurities, and the at least one second-type diffusion region 56 is formed of P-type impurities, fig. 9

Regarding claim 10, Yu discloses the semiconductor device of claim 1, wherein the insulating region 54 of the second well 50 has a structure that surrounds the first well 60, to view in fig. 5.

Regarding claim 19, Yu discloses a method of forming a semiconductor device comprising: forming a first well 60 connected to a pad 10 to which an external pin is connected, the first well 60 including a first-type diffusion region 46 that receives a well

bias voltage; forming a second well 50 adjacent to the first well 60, the second well including an insulating region 54 and at least one second-type diffusion region 56 outside the insulating region 54; and forming a third well 60 adjacent to the second well 50 and including a first-type diffusion region 48 that receives a first voltage, wherein the insulating region 54 inside the second well along with the first-type diffusion region 46 of the first well 60 constitute a bipolar junction transistor, fig. 4, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Yu's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 23, Yu discloses the method of claim 19, wherein the first and third wells are N-wells 50/60, fig. 9.

Regarding claim 24, Yu discloses the method of claim 19, wherein the first-type diffusion regions 46 are formed of N-type impurities, and the at least one second-type diffusion region 56 is formed of P-type impurities, fig. 9.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 2-5, 11-18, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5889309 to Yu et al in view of US 6291303 to Tung.

Regarding claims 2, 4, Yu discloses the semiconductor device of claim 1, wherein the at least one second-type diffusion region 52 outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the second well comprises: a first sub-well arranged (right portion of well 50) between the insulating region 54 and the first well 40 and including the first second-type diffusion region 56; and a second sub-well (left portion of well 50) arranged between the insulating region 54 and the third well 60 and including the second

second-type diffusion region 52, fig. 9, and wherein the insulating region having a first-type diffusion region 54, fig. 9

But, Yu does not disclose the semiconductor device wherein the insulating region is a third sub N-well.

However, Tung discloses a bipolar junction transistor (BJT) in fig. 3A-F wherein at least one second-type diffusion region 318a, column 4 line 24, outside the insulating region 308a, column 3 line 30, comprises a first second-type diffusion region 318a and a second second-type diffusion region 318a, and the well 306a, column 3 line 8, comprises: a first sub-well arranged (right portion of well 306a) between the insulating region 308a and including the first second-type diffusion region 318a; and a second sub-well (left portion of well 306a) and including the second second-type diffusion region 318a, fig. 3F, and wherein the insulating region 308a is a third sub N-well, column 3 line 30, having a first-type diffusion region 316a, column 4 line 15 fig. 3F. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the BJT having a insulating region teaching of Tung with Yu's device, because the additional well around the contact region of the BJT would have increased the gain and efficiency of the BJT as taught by Tung, column 4 lines 44-60.

Regarding claim 3, Yu discloses the semiconductor device of claim 2, wherein the first and second sub-wells of the second well are P-wells, and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well, fig. 9.

Regarding claim 5, Yu discloses the semiconductor device of claim 4, wherein the first voltage is a ground voltage, and the second voltage generates a backward voltage between a base and an emitter of a bipolar junction transistor, fig. 4, the bipolar junction transistor comprising the first-type diffusion region of the first well 60, the second-type diffusion region of the first sub-well 50,

But Yu does not disclose the first-type diffusion region of the third sub-well.

However, as discussed in the above claims 2 and 4, the same reasoning is used with Tung's reference.

With respect to 'a backward voltage between a base and an emitter of the bipolar junction transistor', The structure recited in the Yu's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 11, 18, Yu does not the semiconductor device of claim 1, wherein the third well 60 constitutes a depletion-type MOS transistor.

A recitation of 'a depletion-type MOS transistor' of the claimed invention does not result in a structural difference between the claimed invention and the

prior art, thus claimed invention is only an art recognized suitability for an intended purpose, MPEP 2144.07.

Regarding claim 12, Yu discloses a semiconductor device in fig. 9 comprising: a first N-well 60 connected to a pad 10 to which an external pin is connected, the first N-well 60 including an N-type diffusion region 46 that receives a well bias voltage, and a P-type diffusion region 44, fig. 9, formed in the vicinity of the pad 10; a first P-well 50 adjacent to the first N-well 60, the first P-well 50 including an insulating region 54 and at least one P-type diffusion region 56 that receives a ground voltage outside the insulating region 54; and a second N-well 60 adjacent to the first P-well 50 and including an N-type diffusion region 48 that receives the ground voltage, wherein the insulating region having an N-type diffusion region 54 that receives a control voltage, fig. 9.

But Yu does not disclose the insulating region 54 is a third N-well.

However, Tung discloses a bipolar junction transistor (BJT) in fig. 3A-F comprises a insulating region 308a is a N-well, column 3 line 30, having N-type diffusion region 316a, column 4 line 15. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the BJT having a insulating region teaching of Tung with Yu's device, because the additional well around the contact region of the BJT would have increased the gain and efficiency of the BJT as taught by Tung, column 4 lines 44-60.

Regarding claim 13, Yu discloses the semiconductor device of claim 12, wherein the at least one P-type diffusion region 56 comprises a first P-type diffusion region 56 and a second P-type diffusion region 52, fig. 9, and the first P-well comprises 50: a first

sub-P-well (right portion of 50) located between the insulating region 54 and the first N-well 60 and including the first P-type diffusion region 56; and a second sub-P-well (left portion of 50) located between the insulating region 54 and the second N-well 60 and including the second P-type diffusion region 52.

Regarding claim 14, Yu discloses the semiconductor device of claim 13, wherein the N-type diffusion region 46 of the first N-well 60, the P-type diffusion region 56 of the first sub-P-well, and the N-type diffusion region 54 of the insulating region constitute a bipolar junction transistor which cuts off a current flowing from the first N-well 60 to the second N-well 60.

> The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Yu's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 15, Yu discloses the semiconductor device of claim 14, wherein the control voltage generates a backward voltage between a base and an emitter of the bipolar junction transistor composed of the N-type diffusion region 46 of the first N-well 60, the P-type diffusion region 56 of the first sub-P-well, and the N-type diffusion region 54 of the insulating region.

With respect to 'a backward voltage between a base and an emitter of the bipolar junction transistor', The structure recited in the Yu's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 16, Yu discloses the semiconductor device of claim 12, wherein the well bias voltage applied to the N-type diffusion region of the first N-well is a power supply voltage, fig. 9.

Regarding claim 17, Yu discloses the semiconductor device of claim 12, wherein the insulating region 54 of the first P-well 50 has a structure that surrounds the first N-well 6 (top view), fig. 5.

Regarding claims 20, 22, Yu discloses the method of claim 19, wherein the at least one second-type diffusion region 56 outside the insulating region 54 comprises a first second-type diffusion region 56 and a second second-type diffusion region 52, and the step of forming a second well 40 comprises: forming a first sub-well (right portion of 50) between the insulating region 54 and the first well 60, the first sub-well including the first second-type diffusion region 56; and forming a second sub-well (left portion of 50) between the insulating region 54 and the third well 60, the second sub-well

including the second second-type diffusion region 52, wherein the insulating region having a first-type diffusion region 54.

But, Yu does not disclose the method of forming a semiconductor device wherein the insulating region is a third sub N-well.

However, Tung discloses a method of forming a bipolar junction transistor (BJT) in fig. 3A-F wherein at least one second-type diffusion region 318a, column 4 line 24, outside the insulating region 308a, column 3 line 30, comprises a first second-type diffusion region 318a and a second second-type diffusion region 318a, and the well 306a, column 3 line 8, comprises: a first sub-well arranged (right portion of well 306a) between the insulating region 308a and including the first second-type diffusion region 318a; and a second sub-well (left portion of well 306a) and including the second second-type diffusion region 318a, fig. 3F, and wherein the insulating region 308a is a third sub N-well, column 3 line 30, having a first-type diffusion region 316a, column 4 line 15 fig. 3F. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the BJT having a insulating region teaching of Tung with Yu's device, because the additional well around the contact region of the BJT would have increased the gain and efficiency of the BJT as taught by Tung, column 4 lines 44-60.

Regarding claim 21, Yu discloses the method of claim 20, wherein the first and second sub-wells of the second well are P-wells, and the first voltage is applied to the

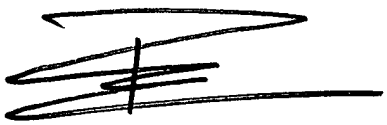
second-type diffusion regions 56 of the first and second sub-wells of the second well, fig. 9.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
Patent Examiner
15 June 2005